What is claimed is:

1. A method of manufacturing a capacitor in semiconductor devices, comprising the steps of:

forming a lower copper electrode on a substrate;

forming a photoresist pattern having a capacitor hole through which the lower copper electrode is exposed;

hardening the surface of the photoresist pattern to form a photoresist hardening layer;

forming a capacitor dielectric film and an upper electrode material layer on the photoresist hardening layer including the capacitor hole;

polishing the upper electrode material layer and the capacitor dielectric film by means of chemical mechanical polishing process to form an upper electrode within the capacitor hole; and

removing the photoresist pattern including the photoresist hardening layer.

2. The method as claimed in claim 1, wherein the photoresist pattern is formed using a photoresist used in a semiconductor manufacture process including silicon-containing resist.

3. The method as claimed in claim 1, wherein the photoresist hardening layer is formed by performing silylation process with the photoresist pattern formed.

4. The method as claimed in claim 3, wherein the silylation process is performed at a temperature of 50 ~ 300℃ using silicon series compounds of HMDS, TMDS and B(DMA)MS.

5. The method as claimed in claim 1, wherein the photoresist hardening layer is surface-treated by means of O_2 ashing process with the photoresist pattern formed.

6. The method as claimed in claim 1, wherein the capacitor dielectric film is formed using oxide, nitride, oxynitride and materials similar to them.

7. The method as claimed in claim 1, wherein the upper electrode material layer is formed using Ti, TiN, Ta, TaN and materials similar to them.